FIG. 20

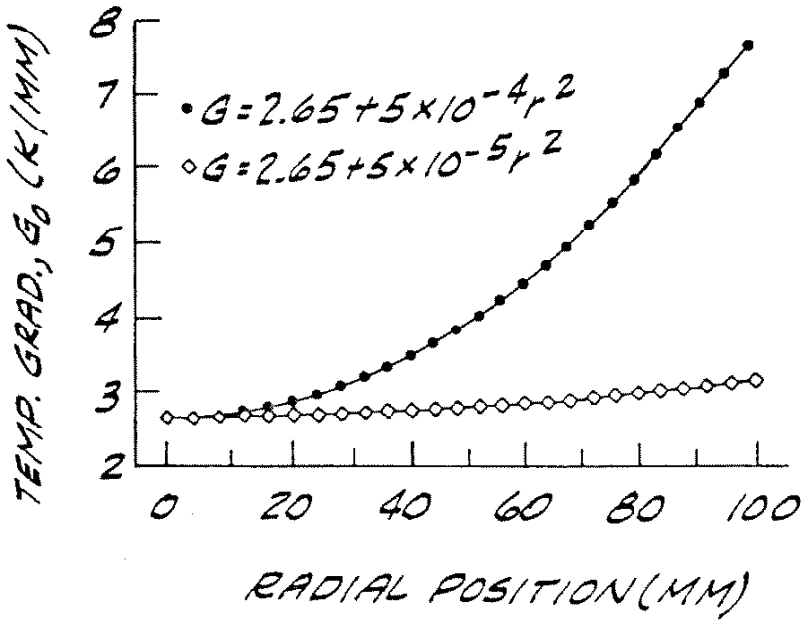

TEMP. GRAD., G_0 (K/MM)
8
7
6
5
4
3
2
• $G = 2.65 + 5 \times 10^{-4} r^2$
◇ $G = 2.65 + 5 \times 10^{-5} r^2$
0
20
40
60
80
100
RADIAL POSITION (MM)

FIG. 21

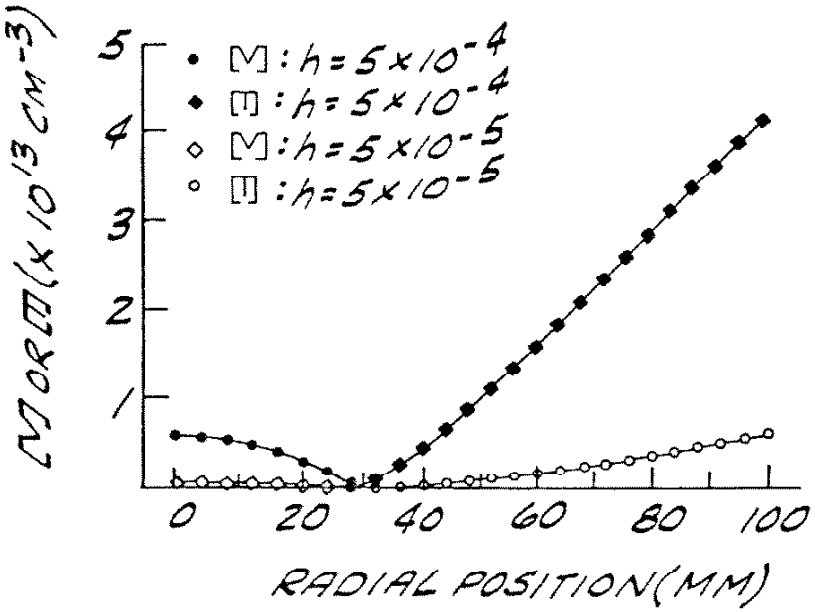

[V] OR [I] ($\times 10^{13}$ CM^{-3})
5
4
3
2
1
• [V] : $h = 5 \times 10^{-4}$
◆ [I] : $h = 5 \times 10^{-4}$
◇ [V] : $h = 5 \times 10^{-5}$
○ [I] : $h = 5 \times 10^{-5}$
0
20
40
60
80
100
RADIAL POSITION (MM)

FIG. 22

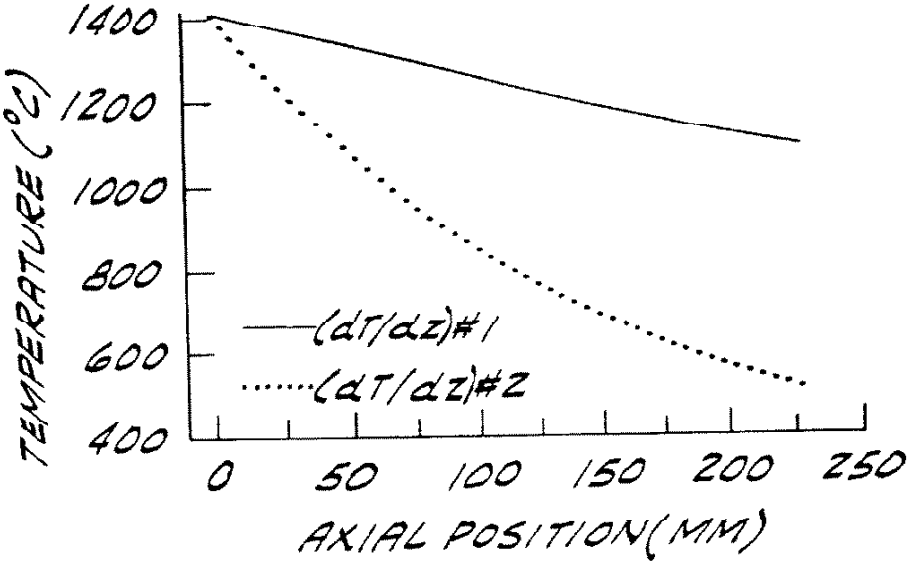

1400
1200
1000
800
600
400
TEMPERATURE (°C)
(dT/dz)#1
(dT/dz)#2
0
50
100
150
200
250
AXIAL POSITION(MM)

FIG. 23

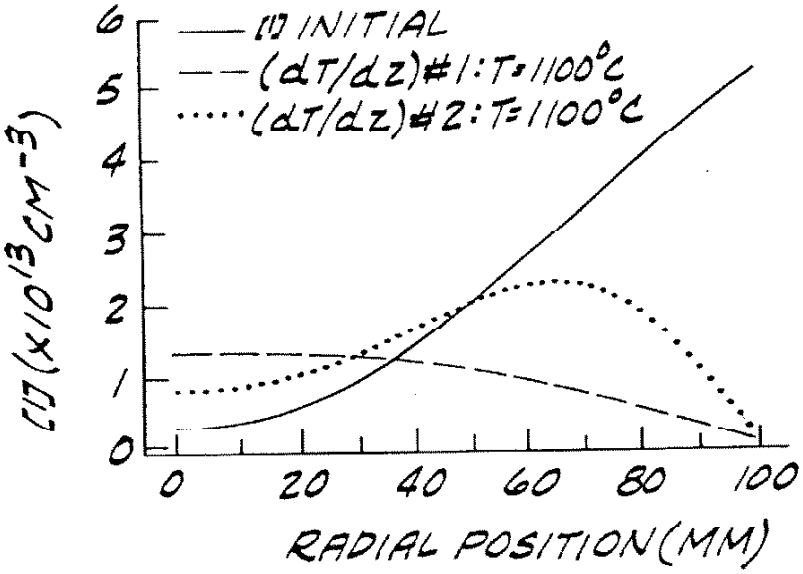

6
5
4
3
2
1
0
[I] (x10^13 CM^-3)
[I] INITIAL
(dT/dz)#1: T=1100°C
(dT/dz)#2: T=1100°C
0
20
40
60
80
100
RADIAL POSITION(MM)

FIG.24

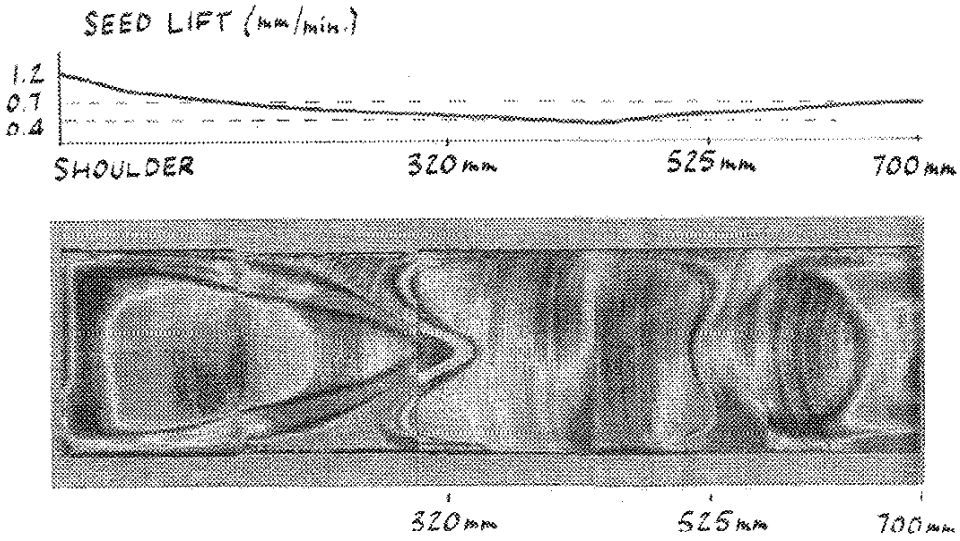

SEED LIFT (mm/min.)
1.2
0.7
0.4
SHOULDER
320 mm
525 mm
700 mm
320 mm
525 mm
700 mm

FIG. 25

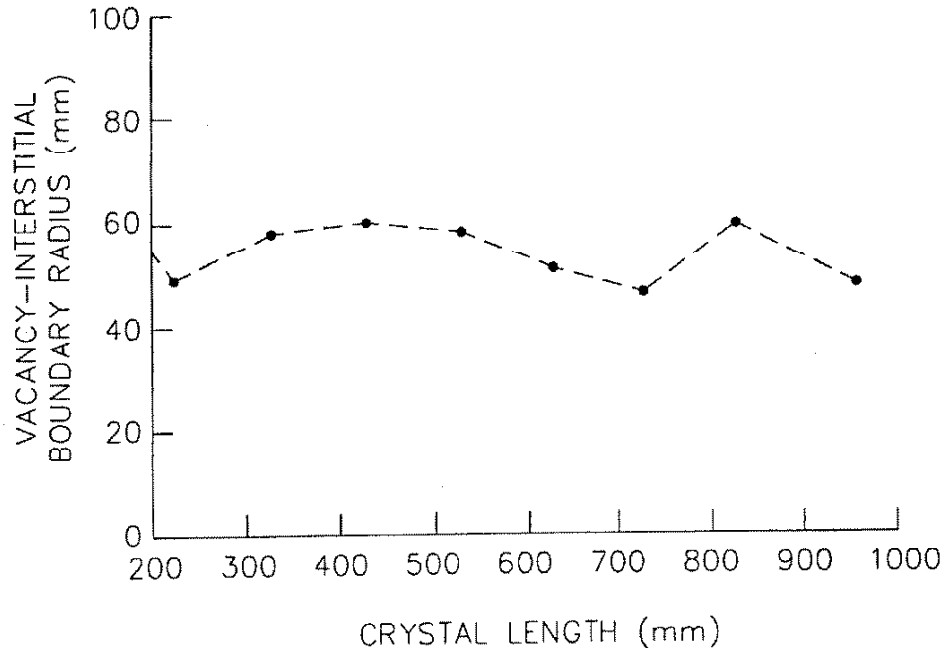

VACANCY-INTERSTITIAL BOUNDARY RADIUS (mm)
100
80
60
40
20
0
200
300
400
500
600
700
800
900
1000
CRYSTAL LENGTH (mm)

FIG. 26A

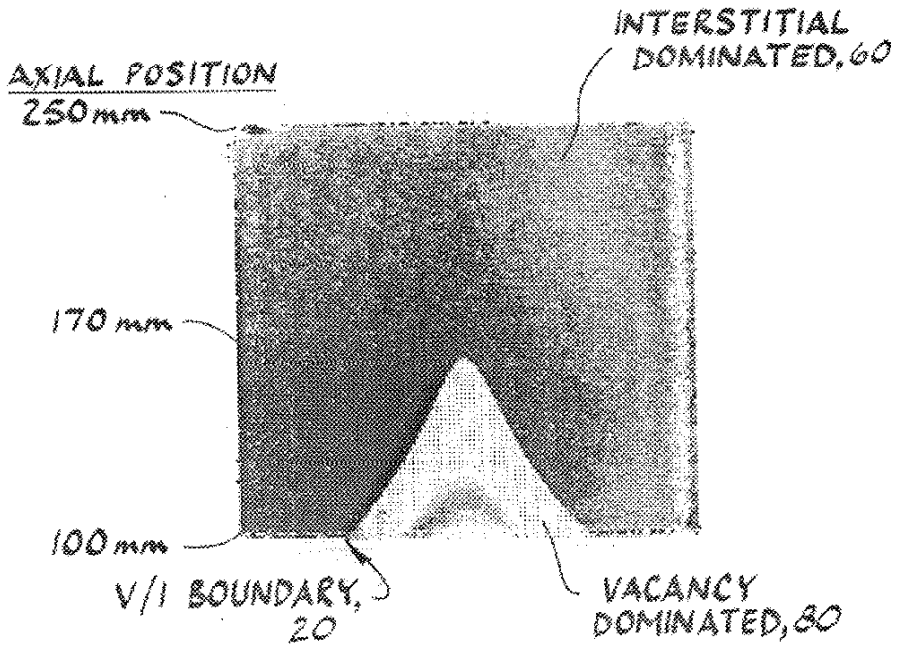
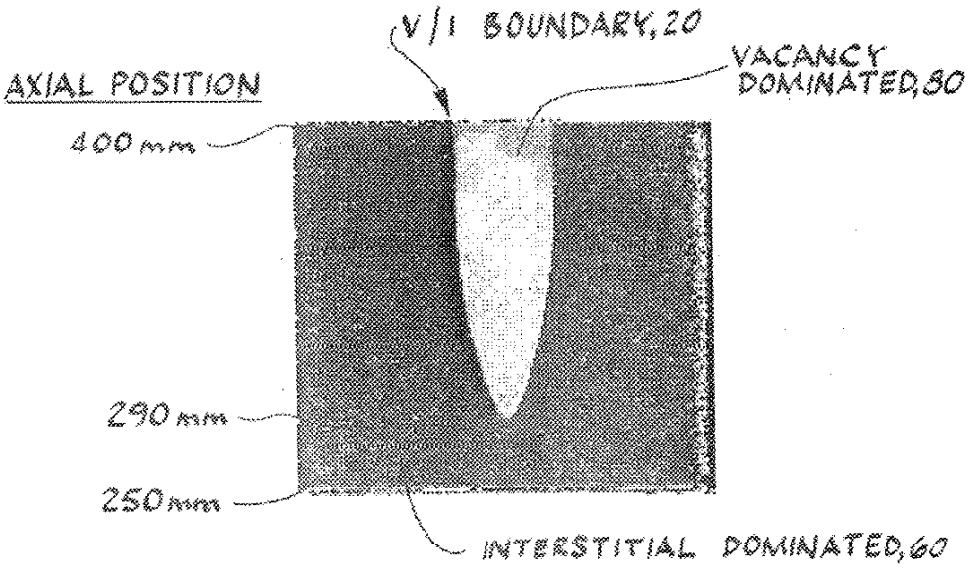

AXIAL POSITION
250 mm
170 mm
100 mm
INTERSTITIAL DOMINATED, 60
V/I BOUNDARY, 20
VACANCY DOMINATED, 80

FIG. 26B


V/I BOUNDARY, 20
VACANCY DOMINATED, 80
AXIAL POSITION
400 mm
290 mm
250 mm
INTERSTITIAL DOMINATED, 60

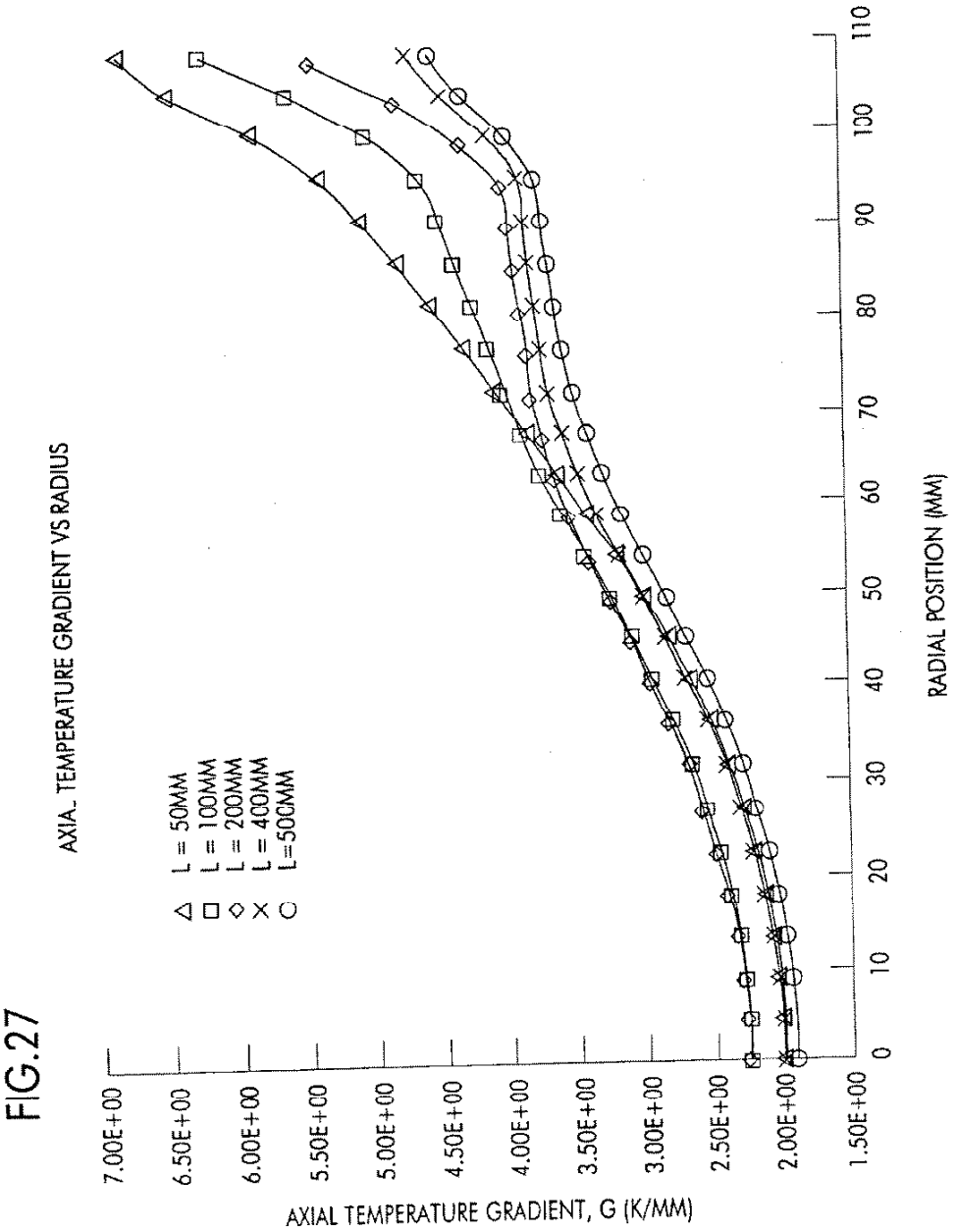

AXIA_ TEMPERATURE GRADIENT VS RADIUS
L = 50MM
L = 100MM
L = 200MM
L = 400MM
L=500MM
AXIAL TEMPERATURE GRADIENT, G (K/MM)
7.00E+00
6.50E+00
6.00E+00
5.50E+00
5.00E+00
4.50E+00
4.00E+00
3.50E+00
3.00E+00
2.50E+00
2.00E+00
1.50E+00
RADIAL POSITION (MM)
0
10
20
30
40
50
60
70
80
90
100
110

FIG.27

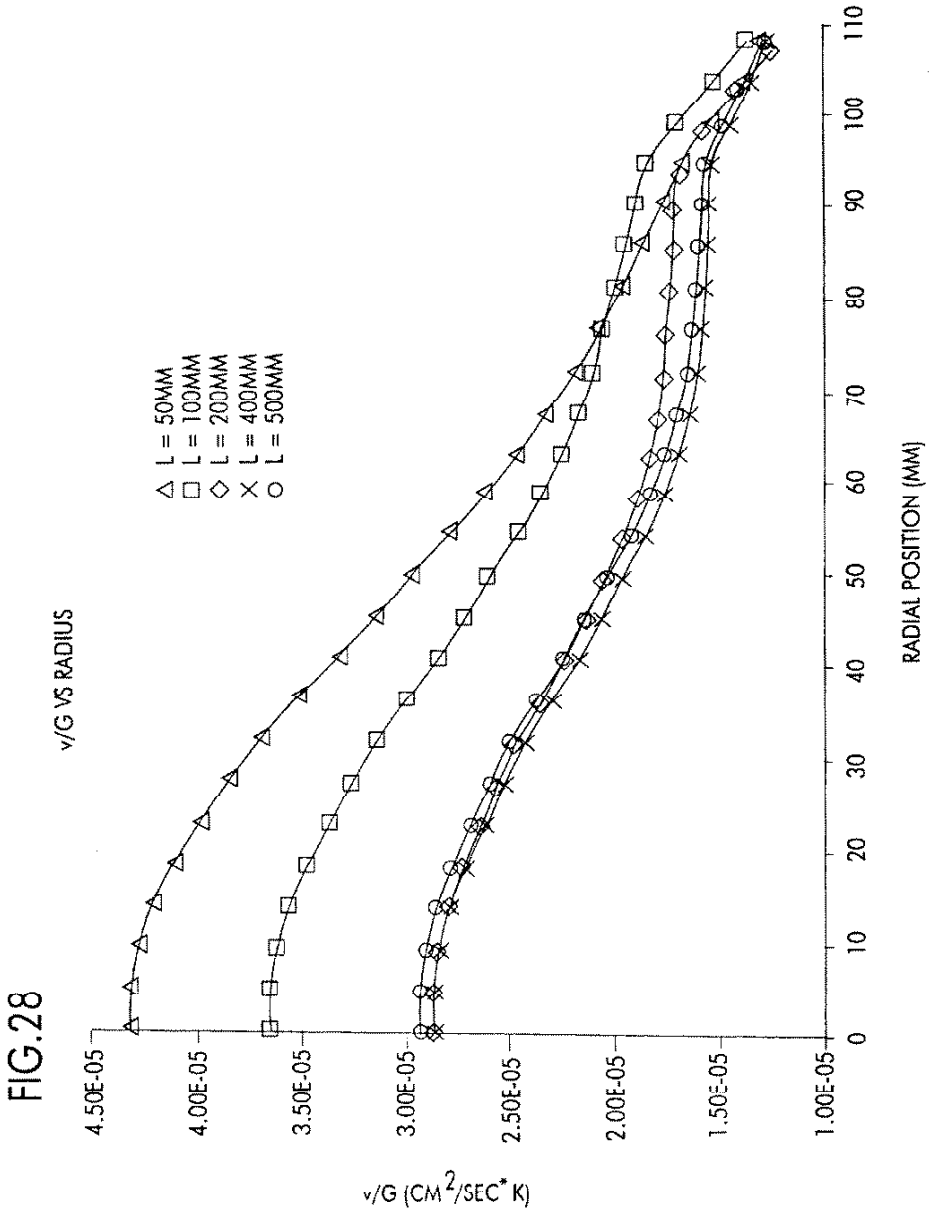

v/G VS RADIUS
L = 50MM
L = 100MM
L = 200MM
L = 400MM
L = 500MM
4.50E-05
4.00E-05
3.50E-05
3.00E-05
2.50E-05
2.00E-05
1.50E-05
1.00E-05
v/G (CM2/SEC* K)
0
10
20
30
40
50
60
70
80
90
100
110
RADIAL POSITION (MM)

FIG.28

FIG.29

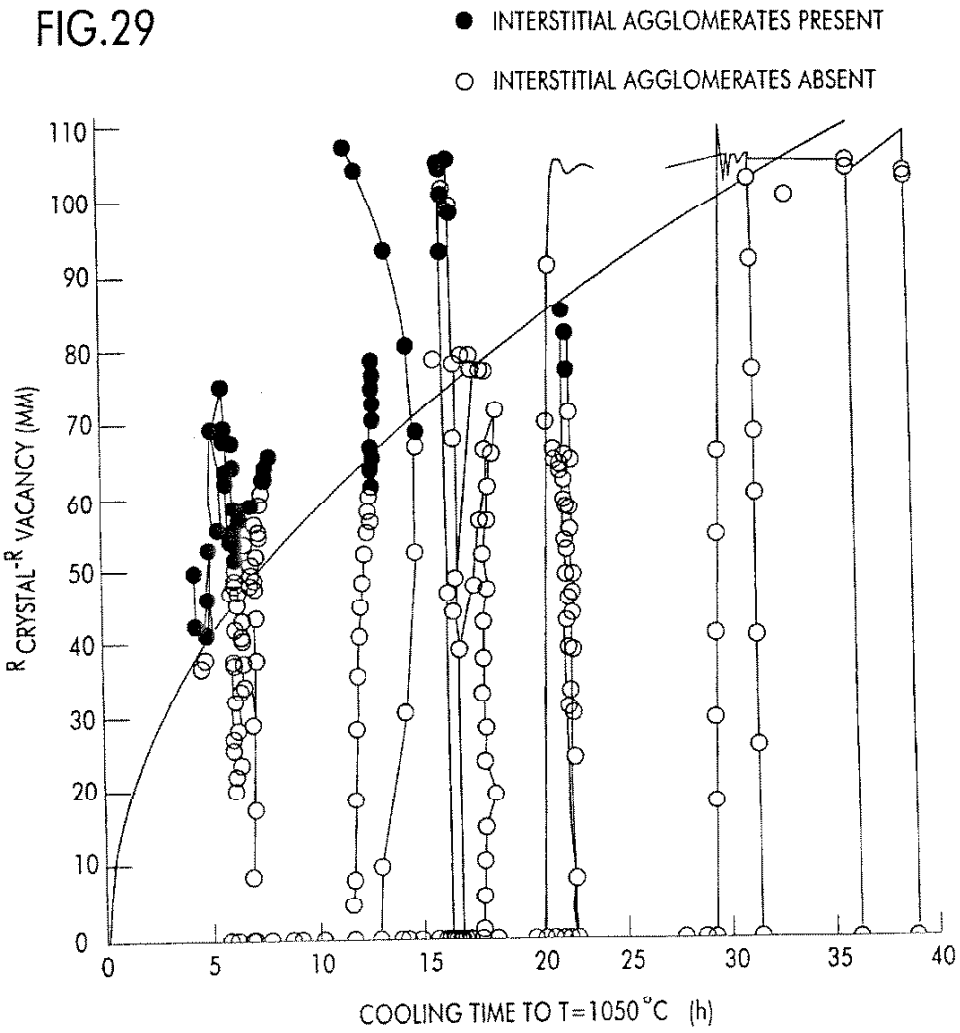

INTERSTITIAL AGGLOMERATES PRESENT
INTERSTITIAL AGGLOMERATES ABSENT
R CRYSTAL-R VACANCY (MM)
110
100
90
80
70
60
50
40
30
20
10
0
0
5
10
15
20
25
30
35
40
COOLING TIME TO T=1050°C (h)

FIG 30

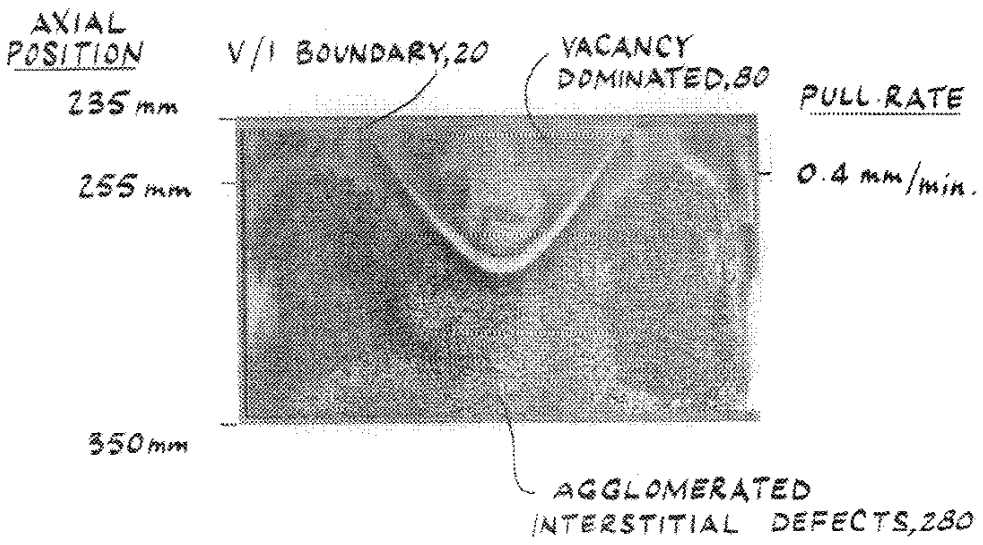

AXIAL POSITION
235 mm
255 mm
350 mm
V/I BOUNDARY, 20
VACANCY DOMINATED, 80
PULL RATE
0.4 mm/min.
AGGLOMERATED INTERSTITIAL DEFECTS, 280

FIG.31

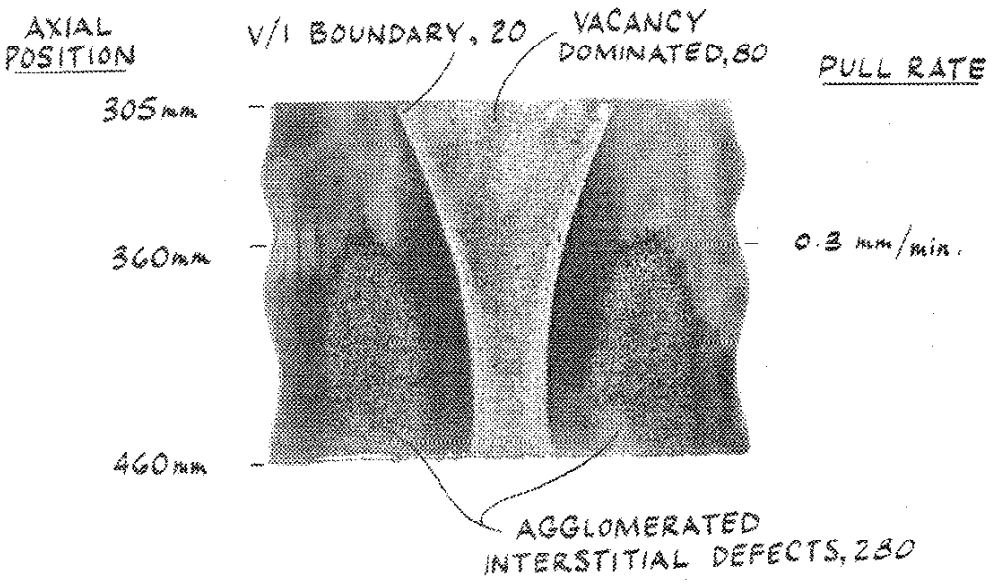

AXIAL POSITION
V/I BOUNDARY, 20
VACANCY DOMINATED, 80
PULL RATE
305mm
360mm
460mm
0.3 mm/min.
AGGLOMERATED INTERSTITIAL DEFECTS, 280

FIG.32

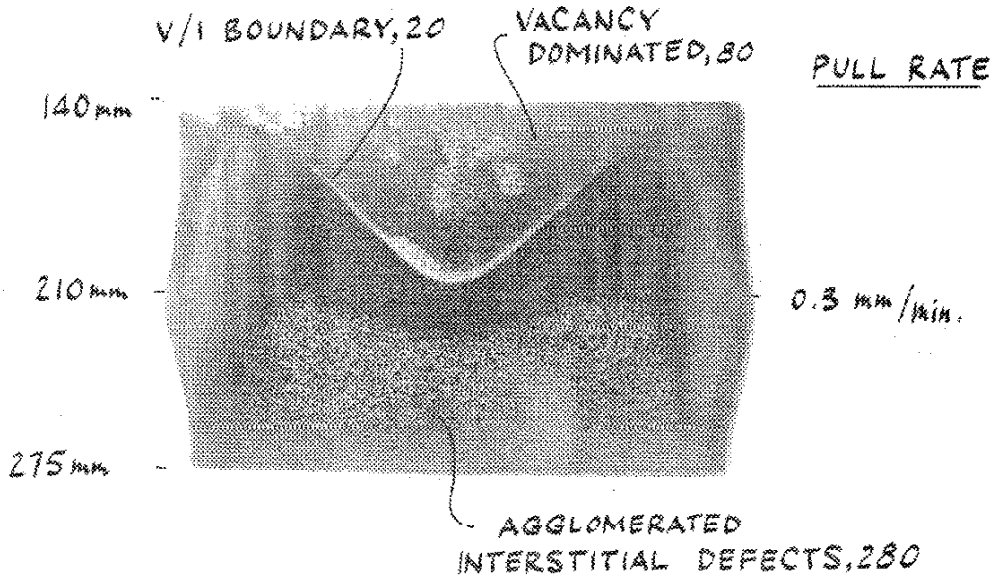
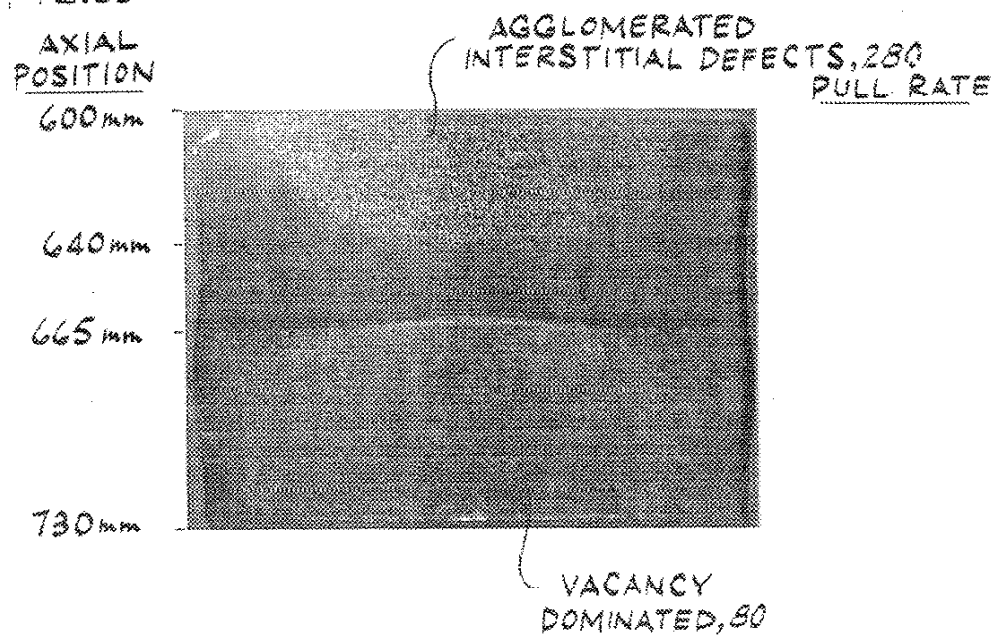

V/I BOUNDARY, 20
VACANCY DOMINATED, 80
PULL RATE
140 mm
210 mm
275 mm
0.3 mm/min.
AGGLOMERATED INTERSTITIAL DEFECTS, 280

FIG.33


AXIAL POSITION
600mm
640mm
665mm
730mm
AGGLOMERATED INTERSTITIAL DEFECTS, 280
PULL RATE
VACANCY DOMINATED, 80

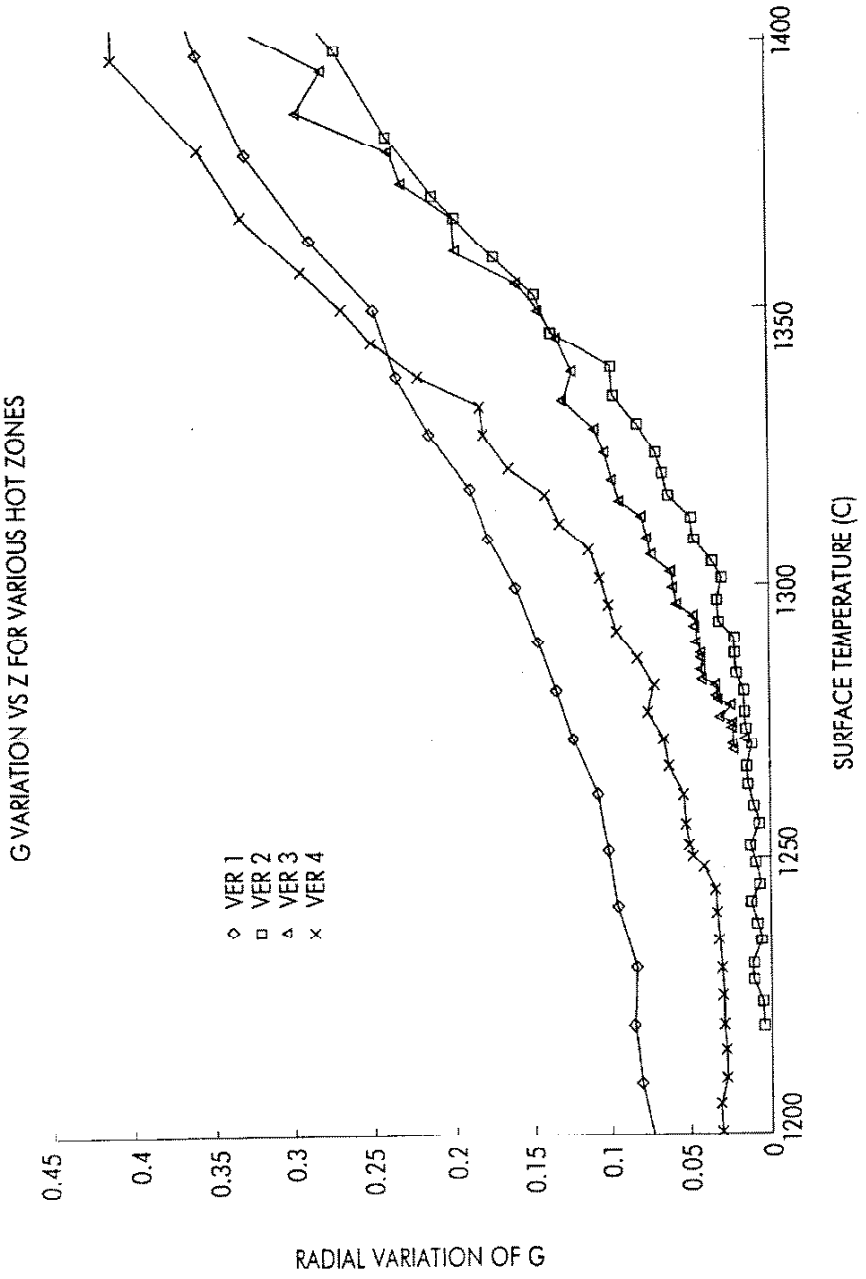

G VARIATION VS Z FOR VARIOUS HOT ZONES
VER 1
VER 2
VER 3
VER 4
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
RADIAL VARIATION OF G
1400
1350
1300
1250
1200
SURFACE TEMPERATURE (C)

FIG.34

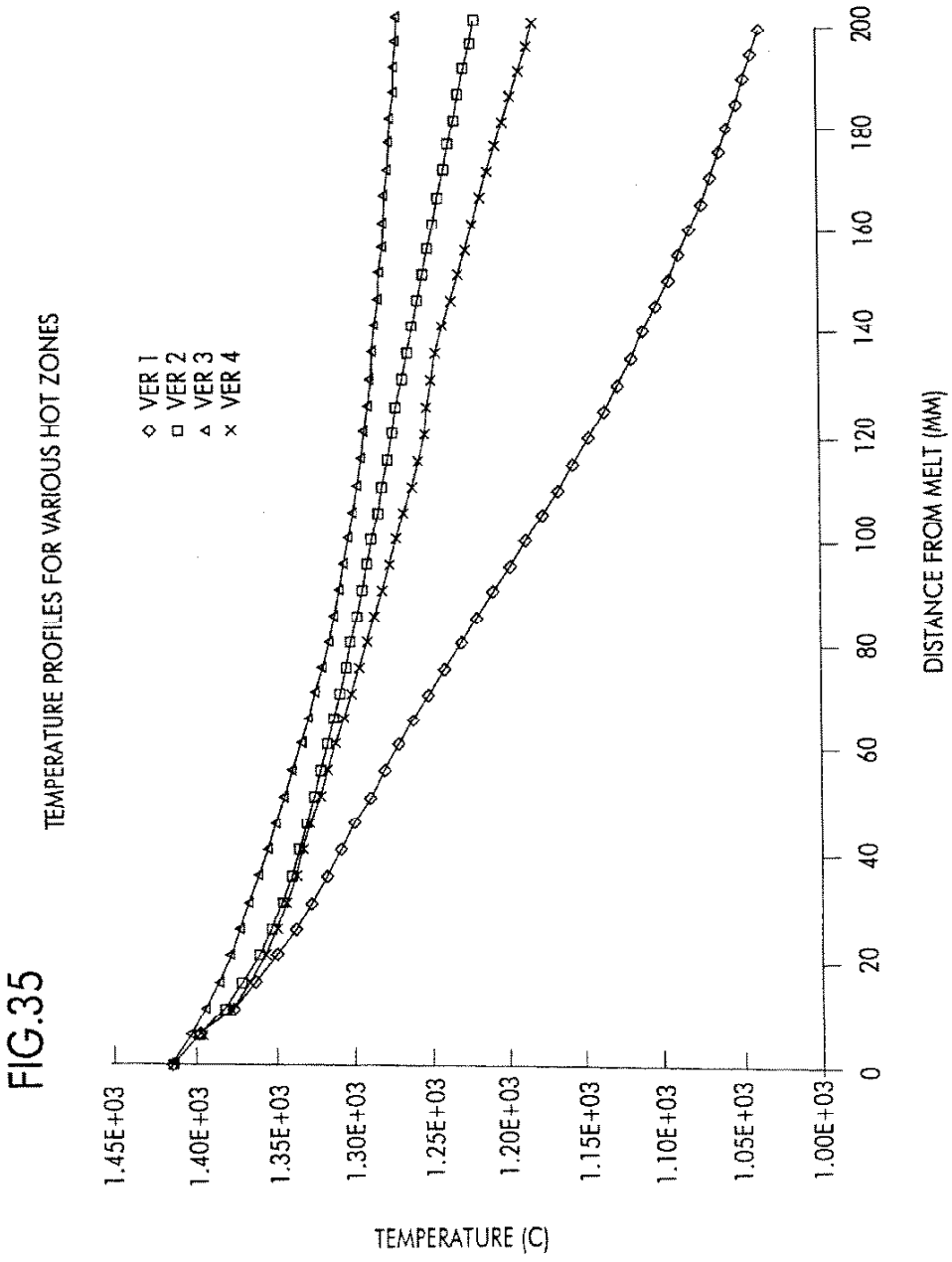

TEMPERATURE PROFILES FOR VARIOUS HOT ZONES
VER 1
VER 2
VER 3
VER 4
1.45E+03
1.40E+03
1.35E+03
1.30E+03
1.25E+03
1.20E+03
1.15E+03
1.10E+03
1.05E+03
1.00E+03
TEMPERATURE (C)
0
20
40
60
80
100
120
140
160
180
200
DISTANCE FROM MELT (MM)

FIG.35

FIG. 36

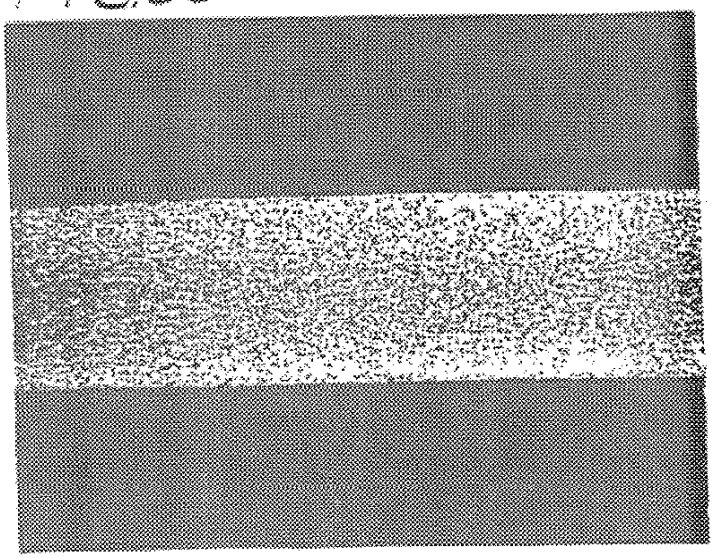


FIG. 37

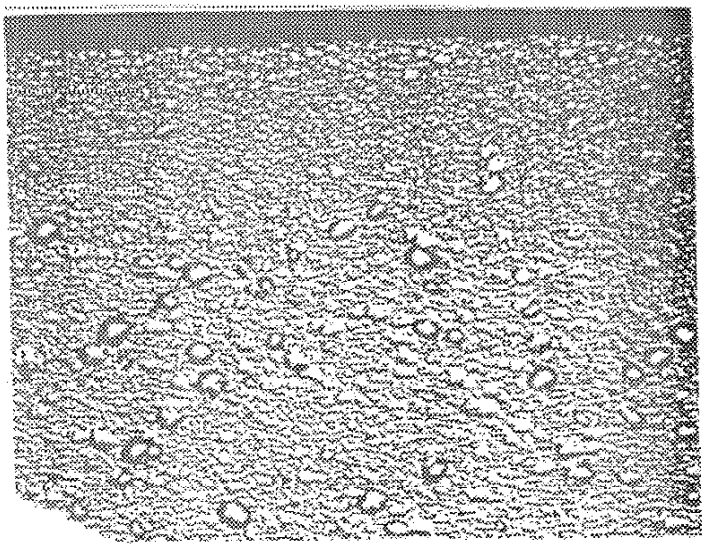


FIG. 38

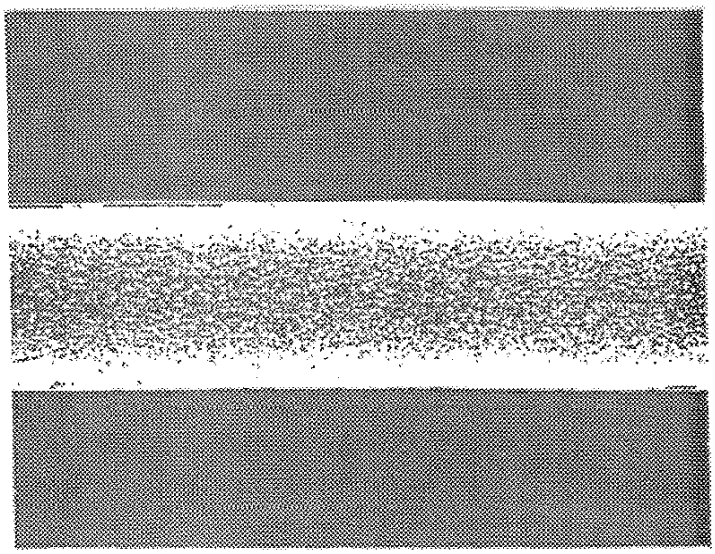


FIG. 39

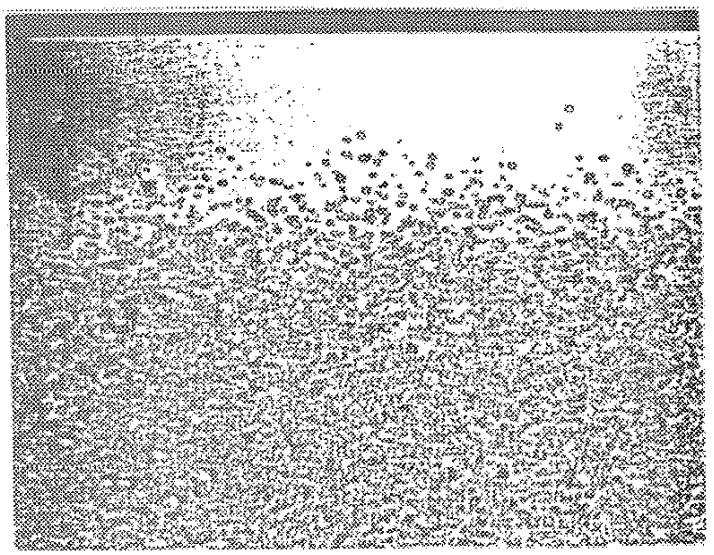


FIG. 40

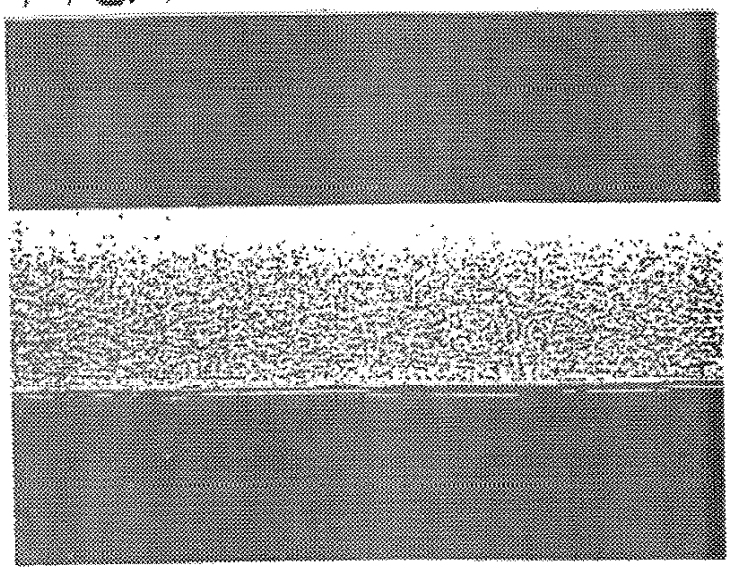
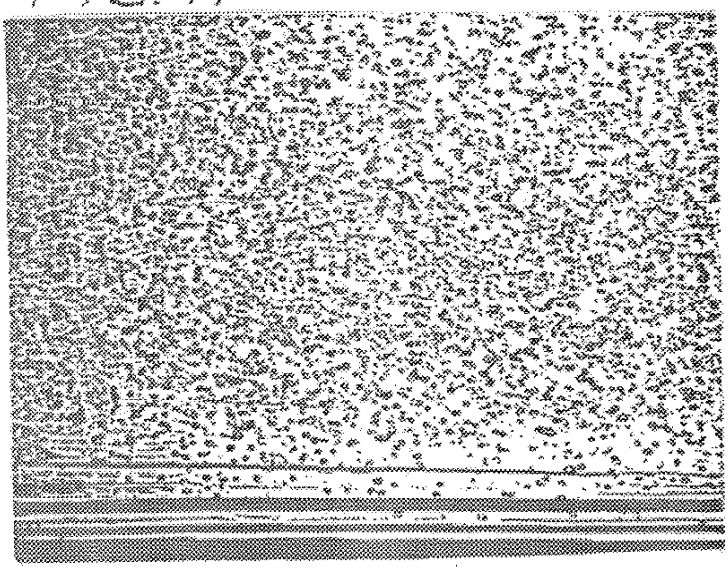


FIG. 41



SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON

REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. provisional application Ser. No. 60/098,902, filed on Sep. 2, 1998.

BACKGROUND OF THE INVENTION

The present invention is directed to a silicon on insulator (SOI) structure having a low defect density device layer. More specifically, the present invention is directed to a SOI structure wherein the device layer is derived from a single crystal silicon wafer which is substantially free of agglomerated intrinsic point defects.

Additionally, the present invention is directed to a SOI structure having a single crystal silicon handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates, upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

A SOI structure generally comprises a handle wafer, a device layer, and an insulating film, (typically an oxide layer) between the handle wafer and the device layer. Generally, the device layer is between 0.5 and 20 micrometers thick. Such a wafer may be prepared using various techniques known in the art. For example, wafer thinning techniques may be used, often referred to as back etch SOI (i.e., BESOI), wherein a silicon wafer is bound to the handle wafer and then slowly etched away until only a thin layer of silicon on the handle wafer remains. (See, e.g., U.S. Pat. No. 5,189,500). Alternatively, a single wafer may be used wherein molecular oxygen ions (O_2^+) or atomic oxygen ions (O^+) are implanted below the surface of the wafer to form an oxide layer. This process is generally referred to as SIMOX (i.e., separation by implantation of oxygen; see, e.g., U.S. Pat. No. 5,436,175 and *Plasma Immersion Ion Implantation For Semiconductor Processing*, Materials Chemistry and Physics 46 (1996) 132–139). Such a process is considered advantageous because it acts to reduce the number of silicon wafers which are consumed, as compared to the more conventional wafer thinning processes, in the preparation of a SOI structure.

SOI structures may be prepared from silicon wafers sliced from single crystal silicon ingots grown in accordance with the Czochralski method. In recent years, it has been recognized that a number of defects in single crystal silicon form during the growth process as the crystal cools after solidification. Such defects arise, in part, due to the presence of an excess (i.e., a concentration above the solubility limit) of intrinsic point defects, which are known as vacancies and self-interstitials. Silicon crystals grown from a melt typically contain an excess of one or the other type of intrinsic point defect, either crystal lattice vacancies or silicon self-interstitials. It has been suggested that the type and initial concentration of these point defects in the silicon are determined at the time of solidification and, if these concentrations reach a level of critical supersaturation in the system and the mobility of the point defects is sufficiently high, a reaction, or an agglomeration event, will likely occur. Agglomerated intrinsic point defects in silicon can severely impact the yield potential of the material in the production of complex and highly integrated circuits, such as those utilizing SOI structures.

Vacancy-type defects are recognized to be the origin of such observable crystal defects as D-defects, Flow Pattern Defects (FPDs), Gate Oxide Integrity (GOI) Defects, Crystal Originated Particle (COP) Defects, crystal originated Light Point Defects (LPDs), as well as certain classes of bulk defects observed by infrared light scattering techniques such as Scanning Infrared Microscopy and Laser Scanning Tomography. Also present in regions of excess vacancies are defects which act as the nuclei for ring oxidation induced stacking faults (OISF). It is speculated that this particular defect is a high temperature nucleated oxygen agglomerate catalyzed by the presence of excess vacancies.

In addition to the above-mentioned vacancy-type defects, it is also believed that agglomerated vacancy defects, or voids, may be the cause of "HF defects" (i.e., metal precipitation defects). HF defects are, like these other vacancy-type defects, considered to be a critical problem with current SOI technology.

Defects relating to self-interstitials are less well studied. They are generally regarded as being low densities of interstitial-type dislocation loops or networks. Such defects are not responsible for gate oxide integrity failures, an important wafer performance criterion, but they are widely recognized to be the cause of other types of device failures usually associated with current leakage problems.

Agglomerated intrinsic point defects can create performance problems for SOI substrates if silicon wafers containing such defects are utilized as the source of the device layer. Performance problems may also result from metallic contaminants present in the handle wafer portion of the SOI structure. During the heat treatments employed by the SOI process, metallic contaminants, present in the handle wafer as a result of cleaning and handling of the SOI structure, may migrate through the silicon matrix until the oxide layer, present between the handle wafer and the device layer, is reached. Although generally speaking these impurities may not pass through the oxide layer and into the device layer, the oxide layer is a preferential site for the precipitation of these impurities. This precipitation acts to disrupt the oxide layer and interfere with the performance of the SOI device.

Accordingly, a need continues to exist for a SOI substrate which contains a device layer which is substantially free of agglomerated intrinsic point defects. Additionally, a need continues to exist for a SOI substrate which contains a handle wafer capable of inhibiting the precipitation of metallic impurities at or near the oxide layer/silicon interface.

SUMMARY OF THE INVENTION

Among the objects of the present invention, therefore, is the provision of a silicon on insulator structure having a device layer containing an axially symmetric region of substantial radial width which is substantially free of defects resulting from an agglomeration of crystal lattice vacancies or silicon self-interstitials; the provision of such a structure having a handle wafer with improved gettering capabilities; the provision of such a structure wherein the handle wafer comprises a silicon wafer which is capable, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process, of forming an ideal, non-uniform depth distribution of oxygen precipitates; and, the provision of such a structure which is less susceptible to the formation of metal precipitate defects during device fabrication.

Briefly, therefore, the present invention is directed to a silicon on insulator structure which comprises (i) a handle wafer, (ii) a single crystal silicon device layer having a central axis, a circumferential edge, a radius extending from

the central axis to the circumferential edge, and a first axially symmetric region which is substantially free of agglomerated intrinsic point defects, and (iii) an insulating layer between the handle wafer and the device layer.

The present invention is further directed to a silicon on insulator structure which comprises (i) a handle wafer, the handle wafer comprising a Czochralski single crystal silicon wafer having two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises a second region of the silicon wafer between the central plane and the first region, the silicon wafer being characterized in that it has a non-uniform distribution of crystal lattice vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer, with the vacancies having a concentration profile in which the peak density of the vacancies is at or near the central plane with the concentration generally decreasing from the position of peak density in the direction of the front surface of the handle wafer, (ii) a single crystal silicon device layer, and (iii) an insulating layer between the handle wafer and the device layer.

The present invention is still further directed to a silicon on insulator structure which comprises (i) a handle wafer, the handle wafer comprising a Czochralski single crystal silicon wafer having two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a denuded zone which comprises the region of the silicon wafer from the front surface to a distance, D_1, of at least about 10 micrometers, as measured in the direction of the central plane, and which contains interstitial oxygen, the silicon wafer being characterized in that the concentration of interstitial oxygen in the denuded zone at a distance equal to about one-half of D_1 is at least about 75% of the maximum concentration of interstitial oxygen in the denuded zone, (ii) a single crystal silicon device layer; and (iii) an insulating layer between the handle wafer and the device layer.

Other objects and features of this invention will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic depiction of the ideal precipitating wafer process.

FIG. **2** is a photograph of a cross-section of a wafer (sample 4–7) which was processed as described in Example 1.

FIG. **3** is a photograph of a cross-section of a wafer (sample 4–8) which was subjected to the series of steps described in Example 1.

FIG. **4** is a photograph of a cross-section of a wafer (sample 3–14) which was subjected to the series of steps described in Example 1.

FIG. **5** is a graph of the log of platinum concentration (atoms/cm^3) versus depth from the surface of a wafer (sample 4–7) which was subjected to the series of steps set forth in Example 1.

FIG. **6** is a photograph of a cross-section of a wafer (sample 3–4) which was subjected to the series of steps set forth in Example 2.

FIG. **7** is a photograph of a cross-section of a wafer (sample 3–5) which was subjected to the series of steps set forth in Example 2.

FIG. **8** is a photograph of a cross-section of a wafer (sample 3–6) which was subjected to the series of steps set forth in Example 2.

FIG. **9** is a photograph of a cross-section of a wafer (sample 1–8) which was subjected to the series of steps set forth in Example 3.

FIG. **10** is logarithmic graph of the number density of bulk microdefects (BMD) versus the partial pressure of oxygen present in the atmosphere during rapid thermal annealing of single crystal silicon wafers in accordance with the ideal precipitating wafer process, as described in Example 4.

FIG. **11** is a graph which shows an example of how the initial concentration of self-interstitials, [I], and vacancies, [V], changes with an increase in the value of the ratio v/G_0, where v is the growth rate and G_0 is the average axial temperature gradient.

FIG. **12** is a graph which shows an example of how ΔG_f, the change in free energy required for the formation of agglomerated interstitial defects, increases as the temperature, T, decreases, for a given initial concentration of self-interstitials, [I].

FIG. **13** is a graph which shows an example of how the initial concentration of self-interstitials, [I], and vacancies, [V], can change along the radius of an ingot or wafer, as the value of the ratio v/G_0 decreases, due to an increase in the value of G_0. Note that at the V/I boundary a transition occurs from vacancy dominated material to self-interstitial dominated material.

FIG. **14** is a top plan view of a single crystal silicon ingot or wafer showing regions of vacancy, V, and self-interstitial, I, dominated materials respectively, as well as the V/I boundary that exists between them.

FIG. **15** is a longitudinal, cross-sectional view of a single crystal silicon ingot showing, in detail, an axially symmetric region of a constant diameter portion of the ingot.

FIG. **16** is an image produced by a scan of the minority carrier lifetime of an axial cut of the ingot following a series of oxygen precipitation heat treatments, showing in detail a generally cylindrical region of vacancy dominated material, a generally annular shaped axially symmetric region of self-interstitial dominated material, the V/I boundary present between them, and a region of agglomerated interstitial defects.

FIG. **17** is a graph of pull rate (i.e., seed lift) as a function of crystal length, showing how the pull rate is decreased linearly over a portion of the length of the crystal.

FIG. **18** is an image produced by a scan of the minority carrier lifetime of an axial cut of the ingot following a series of oxygen precipitation heat treatments, as described in Example 6.

FIG. **19** is a graph of pull rate as a function of crystal length for each of four single crystal silicon ingots, labeled 1–4 respectively, which are used to yield a curve, labeled v*(Z), as described in Example 6.

FIG. **20** is a graph of the average axial temperature gradient at the melt/solid interface, Go, as a function of radial position, for two different cases as described in Example 7.

FIG. **21** is a graph of the initial concentration of vacancies, [V], or self- interstitials, [I], as a function of radial position, for two different cases as described Example 7.